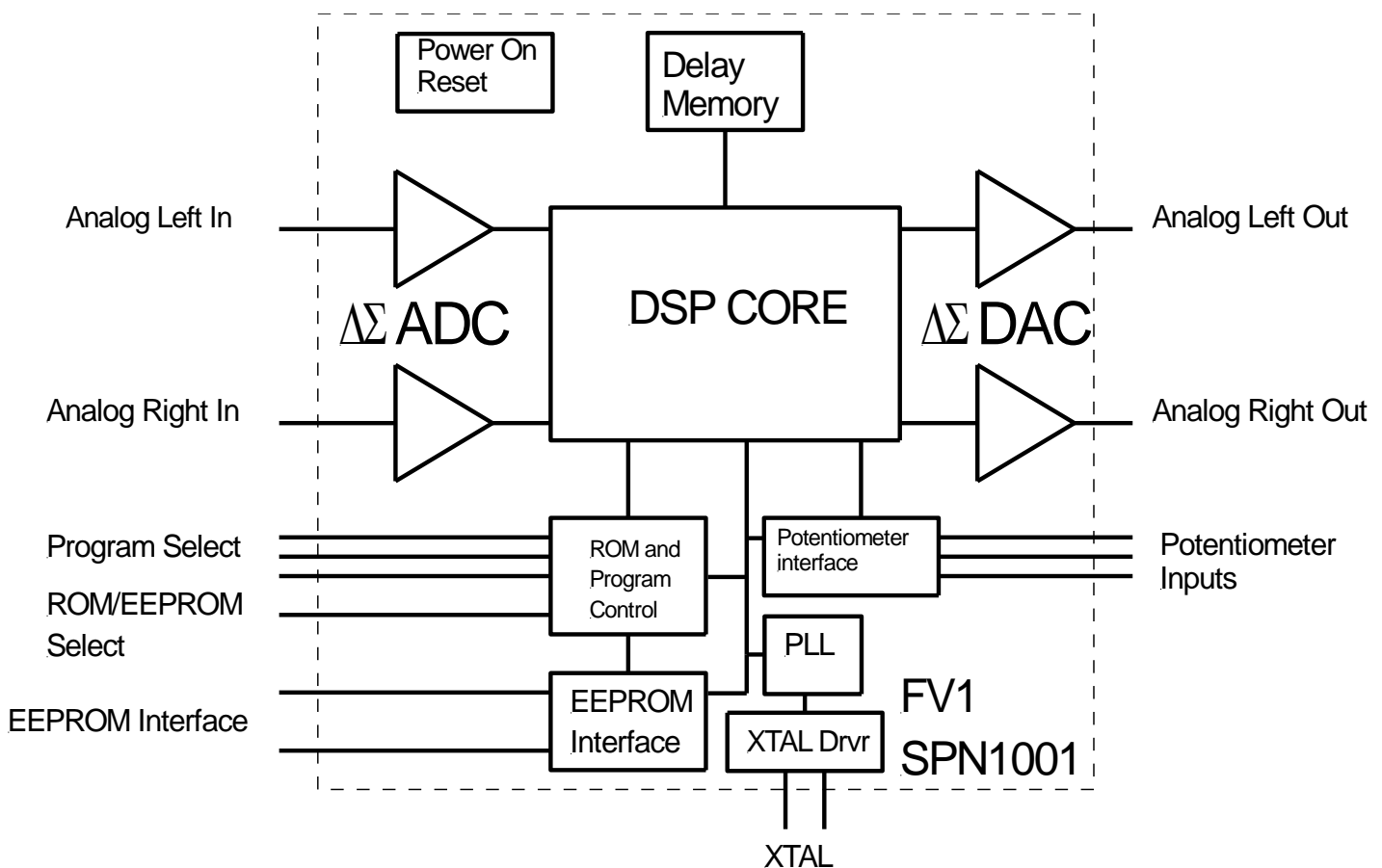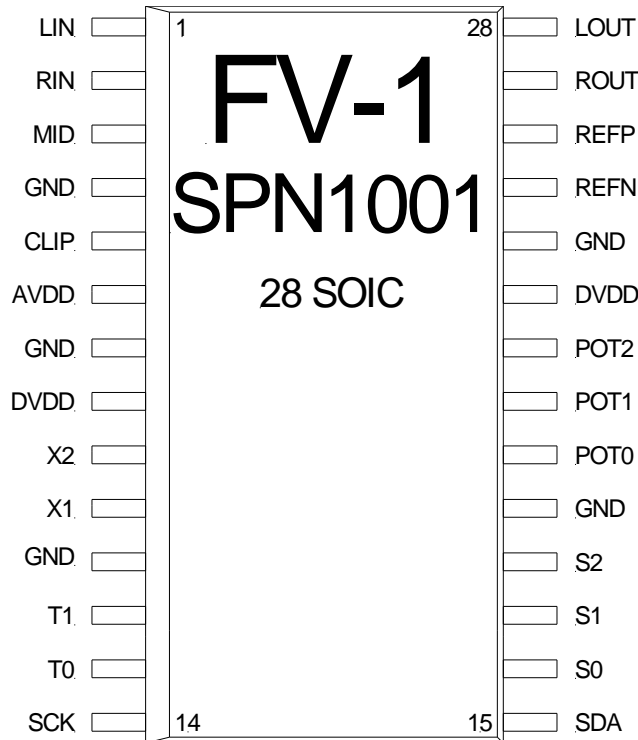## FEATURES

- Integrated stereo ADC and DAC
- 8 internal demonstration programs + 8 external programs
- Easy customization with external EEPROM
- 3 potentiometer inputs for real-time parameter adjustment
- 3.3V operation
- 6 MIPS operation at Fs=48KHz
- 128 instructions/sample clock
- 32K words of delay RAM
- Internal PLL for Fs input clock
- Integrated Power-On-Reset circuit
- LOG and EXP instructions for dynamics
- Green assembly/RoHS compliant

APPLICATIONS

- Guitar Amps
- Mixers
- Effects Equipment
- Karaoke
- Consumer electronics
- Car audio
- Active loudspeaker crossover and flattening
- Industrial processes

```
        LIN  ┌──┐    1              28   ┌──┐  LOUT
        RIN  ┌──┐                        ┌──┐  ROUT
        MID  ┌──┐    FV-1                ┌──┐  REFP
        GND  ┌──┐    SPN1001             ┌──┐  REFN
       CLIP  ┌──┐                        ┌──┐  GND
       AVDD  ┌──┐    28 SOIC             ┌──┐  DVDD
        GND  ┌──┐                        ┌──┐  POT2
       DVDD  ┌──┐                        ┌──┐  POT1
         X2  ┌──┐                        ┌──┐  POT0
         X1  ┌──┐                        ┌──┐  GND
        GND  ┌──┐                        ┌──┐  S2
         T1  ┌──┐                        ┌──┐  S1
         T0  ┌──┐                        ┌──┐  S0
        SCK  ┌──┐   14             15    ┌──┐  SDA
```

Pin	Name	Description
1	LIN	Left analog in
2	RIN	Right analog in
3	MID	Mid reference
4	GND	Ground
5	CLIP	Clip LED output
6	AVDD	Analog power (3.3V)
7	GND	Ground
8	DVDD	Digital power (3.3V)
9	X2	Crystal oscillator input
10	X1	Crystal oscillator input
11	GND	Ground
12	T1	Tie to GND for normal operation
13	T0	0: Use internal ROM programs, 1: Use programs from external EEPROM
14	SCK	EEPROM clock (Internal pull up)
15	SDA	EEPROM data (Internal pull up)
16	S0	Program select LSB
17	S1	Program select
18	S2	Program select MSB
19	GND	Ground
10	POT0	Potentiometer 0 analog input
21	POT1	Potentiometer 1 analog input
22	POT2	Potentiometer 2 analog input
23	DVDD	Digital power (3.3V)
24	GND	Ground
25	REFN	Negative reference
26	REFP	Positive reference
27	ROUT	Right analog out
28	LOUT	Left analog out

Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
A_{VDD}	Analog supply voltage	-0.5	3.5	V
D_{VDD}	Digital supply voltage	-0.5	3.5	V
A_{VI}	Analog input voltage range	-0.5	AVDD+0.5	V
D_{VI}	Digital input voltage range	-0.5	DVDD+0.5	V
I_{IC}	Input signal current		±20	mA
I_{OC}	Output clamp current		±20	mA
I_O	Continuous output current		±20	mA
	Continuous current through VDD or GND		±100	mA
	Maximum power dissipation		300	mW
	Storage temperature range	-50	150	°C

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not guaranteed. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

A_{VDD}	Analog supply voltage	3.3V
D_{VDD}	Digital supply voltage	3.3V
REFP	Positive reference	3.3V
REFN	Negative reference	0V
T_{OP}	Operating temperature	0 – 70 °C

Electrical Characteristics (X1, X2 = 32768Hz crystal, DVDD=AVDD=REFP=3.3V, REFN=0v, measurements over 20-16Khz band)

Characteristic	Min	Typ	Max	Units
Analog input impedance	80		120	KΩ
Analog output impedance	50		200	Ω
Allowable load resistance	10			KΩ
Maximum input signal level	2.6		3.0	V_{P-P}
Maximum output signal level	2.6		3.0	V_{P-P}
Channel gain mismatch			0.2	dB
ADC equivalent input noise (A weighted)		-97	-93	dB
DAC output noise (A weighted)		-97	-93	dB
THD (1KHz, -1db from clipping)		0.015	0.03	%
ADC-DAC HF response (-3dB)	14.5		15.5	KHz
Passband flatness			±0.5	dB
Total internal memory delay (@32.768KHz sample rate)			1.0	seconds
Potentiometer control input impedance	10		20	MΩ
X1, X2 internal capacitance	8		15	pF
X1, X2 internal bias resistance	7		14	MΩ
Supply current (AVDD + DVDD)	40	55	70	mA
REFP supply current	30		50	µA
SDA and SCK internal pull up - Typical	3.75			KΩ

General Description

The Spin Semiconductor FV-1 is a complete reverb solution in a single IC. With integrated stereo ADC and DACs, the FV-1 can be treated like any other analog component in your products signal path.

The FV-1 can access a total of 16 programs, 8 programs are built in to the internal ROM and the designer may elect to connect a serial EEPROM with 8 additional programs. By using an external EEPROM, the designer can distinguish his product from others by creating a custom program set without the need for a microprocessor in the system.

With 3 potentiometer inputs, programs may have real time variable parameters such as decay time in a reverb, rate and depth in a chorus or frequency in a filter. These inputs are available as coefficients to your program and may be used independently of each other.

The rich instruction set allows users to program effects of all kinds. With instructions like LOG and EXP, users can easily program audio expansion and compression routines. Integrated digital LFOs and ramp generators allow for programming chorus, flange and pitch shift.

A complete development system including assembler and development board with USB interface are available from Spin Semiconductor. The assembler and instruction set documentation are available free from the Spin web site along with example code that may be freely used in your product.

ROM Programs

The FV-1 includes 8 programs in the internal ROM, these programs and the assigned potentiometer input controls are detailed in Table 1.

Table 1 - ROM Programs

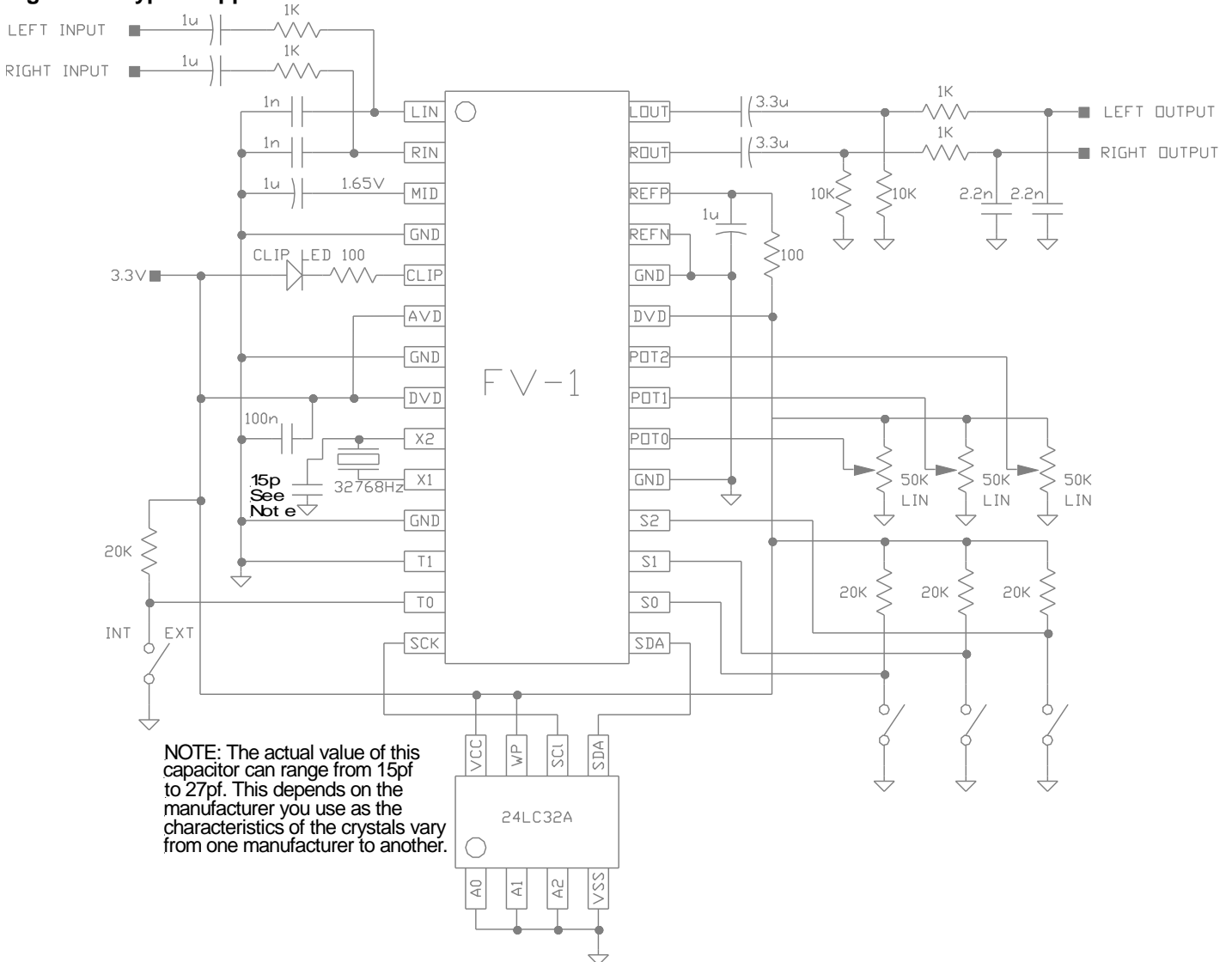| Prg #	Description	POT0	POT1	POT2
0	Chorus-reverb	Reverb mix	Chorus rate	Chorus mix
1	Flange-reverb	Reverb mix	Flange rate	Flange mix
2	Tremolo-reverb	Reverb mix	Tremolo rate	Tremolo mix
3	Pitch shift	Pitch +/-4 semitones	-	-
4	Pitch-echo	Pitch shift	Echo delay	Echo mix
5	Test	-	-	-
6	Reverb 1	Reverb time	HF filter	LF filter
7	Reverb 2	Reverb time	HF filter	LF filter

DSP Core

The DSP core of the FV-1 provides many advanced features and instructions that allow you to create advanced programs to make your product stand out. The DSP core consists of the MAC/ALU where all math and logic instructions take place, the LOG and EXP blocks that perform the log and exponential functions, a 32-register bank separate from the delay RAM and LFO and ramp generators that can offset memory addressing.

A complete list and description of instructions is available in the assembly language manual that is included on the CD in the development kit or may be downloaded from the Spin Semiconductor web site.

Typical Application

The FV-1 is extremely easy to include in any audio system, but certain details should be considered. For all practical purposes, the FV-1 can be treated as an analog part. Although the FV-1 is fully digital internally, it has been designed with internal power supply bypassing and careful attention to signal pin protection devices so that only a clean power supply and expected analog techniques are required at the PCB level.

Figure 1 – Typical application

NOTE: The actual value of this capacitor can range from 15pf to 27pf. This depends on the manufacturer you use as the characteristics of the crystals vary from one manufacturer to another.

The inputs should be conducted through coupling capacitors, as the inputs are internally biased to a VDD/2 potential. The input signals should be led through 1K resistances with 1nF capacitors directly to ground as close as possible to the input pins. These bypass capacitors should be of good quality, either film capacitors or NP0 (COG) ceramic. The purpose of

this input bypassing is to remove any high frequency noise from the input signals, and to provide a low impedance at very high frequencies.

The outputs may contain out of band noise that can be more fully removed through the use of a two-pole active filter, but for most applications this noise is both inaudible and of no consequence to following circuitry. A simple RC filter is sufficient to remove any high frequency components, if required.

The output mute circuit, internal to the device, inserts a 100K ohm resistance in series with output pins during device power-up, which allows the output coupling capacitors to slowly become biased to the nominal output voltage of VDD/2. The load resistance on the outputs should be no less than 10K ohms so as to not overload the output drivers, and the coupling capacitor should have a time constant with the load resistance of about 20 to 50ms. The power up delay will be approximately 0.5 to 1 second, depending on crystal properties.

The clip LED is optional, but will flash for approximately 30mS if the internal ADC or the DAC are driven to within a few tenths of a dB of full scale. Any overflow from internal processing that does not produce a near full scale output will not light the clip LED.
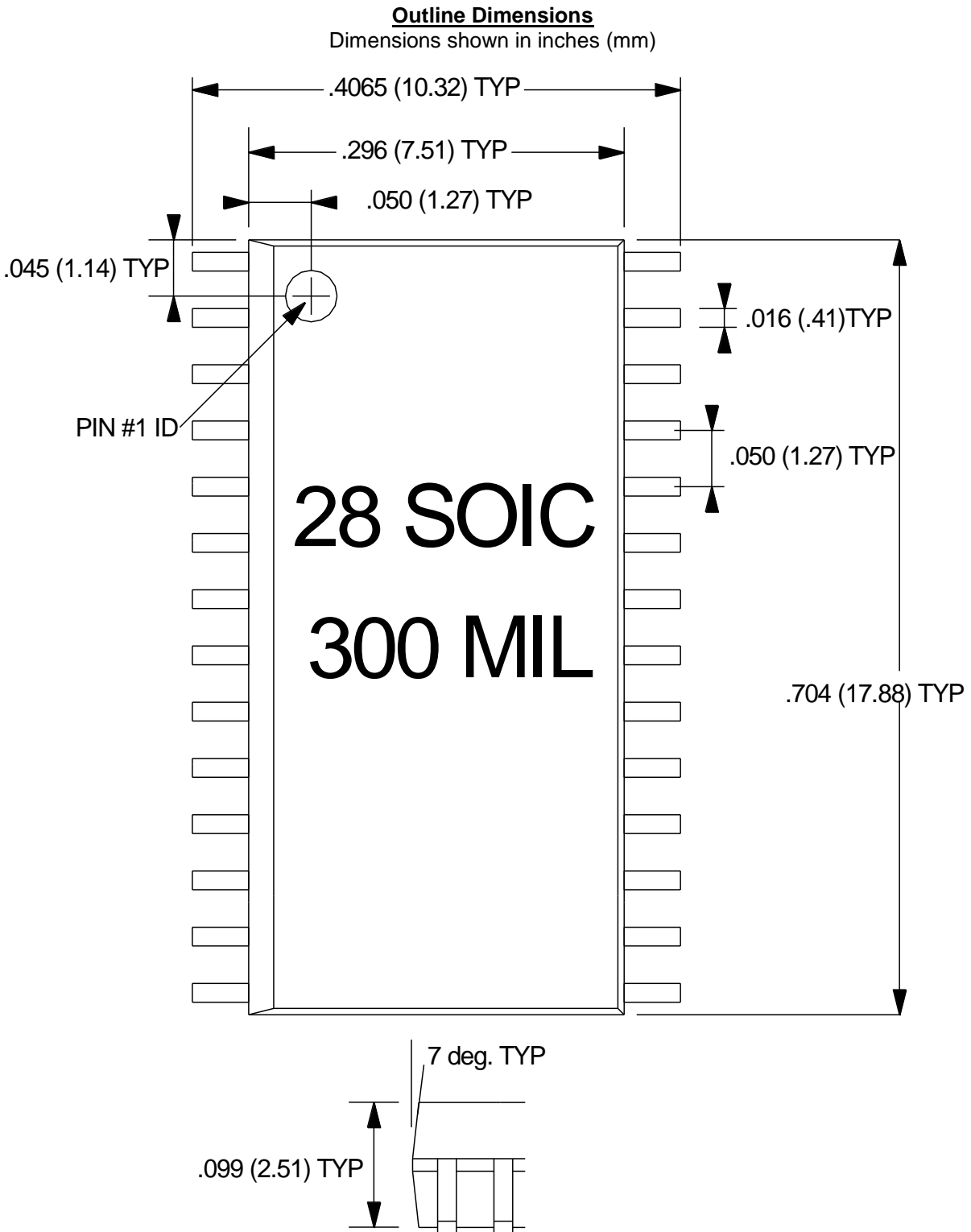
Digital power should be bypassed with a ceramic capacitor to ground with very short leads to the part. Ideally, the design will be onto a double sided PCB with the lower layer as a solid pour, connected to ground. This provides a convenient low inductance connection for bypass capacitors through vias. A single sided PCB can be used provided that a large ground area is included beneath the chip and surface mount bypass capacitors are connected from supply pins to this ground as close to the chip as possible.

Likewise, the REFP and REFN pins should have a bypass cap attached close to the part, with a resistor to supply from VDD. The current drawn by the REFP terminal is small, on the order of 30uA, so there will be only a slight voltage drop across the reference series resistor. The input and output signal levels however, will be a function of the potential across the REFP and REFN pins. Be careful to not make the series filter resistor between VDD and the REFP pin too large, or signal levels will be affected.

The input resistance of the potentiometer control inputs is on the order of 10 megohms, and these terminals are quite resistant to noise. No bypass capacitors should be required on these terminals. If not required, these terminals may be left open, or if the program includes the use of a potentiometer function, it may be connected to MID if a centered potentiometer position is desired, but an actual control is not intended in the design.

The crystal oscillator is designed for the standard 32768 Hz watch crystal, as this is particularly inexpensive, but any logic level clock source can be attached to the X1 terminal directly. The sample rate of the system will be at this applied rate. At 32768Hz, the ADC and DAC bandwidth will be 15KHz, at a clock frequency of 48KHz, the bandwidth will expand to beyond 20KHz. Watch crystals have a very high Q factor, and require significant time to develop full level oscillation. All support components for the crystal are included internal to the device, including a 10Meg bias resistor and two 12pF capacitors. The lead length however, between the crystal and the part must be as short as possible. Further, beware that the loading of a scope probe on the X1 pin may cause the oscillator to stop. If you wish to check the oscillator's operation, use X2 as a measurement point. Depending on the supplier of the crystal there can be a startup problem with the crystal, it is recommended that all designs include a 15pf capacitor between X2 and ground.

The use of an external EEPROM is optional, and in the case of designs that do not make use of this expansion option, the SCK and SDA pins may be left open. T1 however must be grounded, and T0 must be connected to ground (internal programs) or VDD (EEPROM programs).

Outline Dimensions
Dimensions shown in inches (mm)

.4065 (10.32) TYP

.296 (7.51) TYP

.050 (1.27) TYP

.045 (1.14) TYP

.016 (.41)TYP

.050 (1.27) TYP

PIN #1 ID

28 SOIC

300 MIL

.704 (17.88) TYP

7 deg. TYP

.099 (2.51) TYP

Notice

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